

FAST RISETIME REVERSE BIAS PULSE FAILURES IN SiC PN JUNCTION DIODES

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Abstract

SiC-based high temperature power devices are being developed for aerospace systems which require high reliability. To date, it has necessarily been assumed that the breakdown behavior of SiC pn junctions will be similar to highly reliable silicon-based pn junctions. Challenging this assumption, we report the observation of anomalous unreliable reverse breakdown behavior in moderately doped ($2\text{-}3 \times 10^{17} \text{ cm}^{-3}$) small-area 4H- and 6H-SiC pn junction diodes at temperatures ranging from 298 K (25 °C) to 873 K (600 °C). We propose a mechanism in which carrier emission from un-ionized dopants and/or deep level defects leads to this unstable behavior.

INTRODUCTION

The inherent physical properties of silicon carbide (SiC) appear to be extremely well suited for power semiconductor electronic devices. Theoretical appraisals of the characteristics and applications of SiC power devices have suggested that once silicon carbide technology matures sufficiently to overcome some developmental obstacles, SiC may supplant silicon in many high-power electronic applications (Baliga, 1994; Bhatnagar and Baliga, 1993). However, these analyses are primarily based on the numerical substitution of SiC physical properties into existing semiconductor device models. These models have limitations however, as they clearly do not take into account all behaviors of an actual SiC device. One behavior crucial to power device reliability that has necessarily been assumed to date is that the breakdown behavior of SiC pn junctions will (after technology improvements eliminate all crystalline defects such as micropipes) be similar to silicon-based pn junctions. Silicon pn junctions are highly reliable because they exhibit stabilizing properties such as positive temperature coefficient of breakdown voltage (Bell Laboratories, 1984; Ricketts et al., 1976; Sze, 1981). The experimental work presented in this paper casts some doubt upon the presumption of silicon-like breakdown behavior for all SiC pn junctions.

EXPERIMENTAL

Device Fabrication & DC Testing

The SiC homoepilayer structure shown in Figure 1 was grown at NASA Lewis on substrates cut from commercially available p^+ 4H and 6H silicon-face SiC substrates polished 3° to 4° off the (0001) SiC basal plane. The growth and device fabrication procedures used are described elsewhere (Neudeck et al., 1994). Processing of the 4H and 6H samples was done in parallel, with pattern definitions, E-beam deposited metallizations (Al etch mask, Au contacts), etches (RIE), and oxidations (4 hr., 1423 K, wet O_2) being done simultaneously.

Room-temperature 1 MHz capacitance-voltage measurements on large-area diodes estimated the $0.6 \mu\text{m}$ thick n-layer doping at $2 \times 10^{17} \text{ cm}^{-3}$ and $3 \times 10^{17} \text{ cm}^{-3}$ for the 4H and 6H devices, respectively. Over 50 devices were dc tested at room temperature,

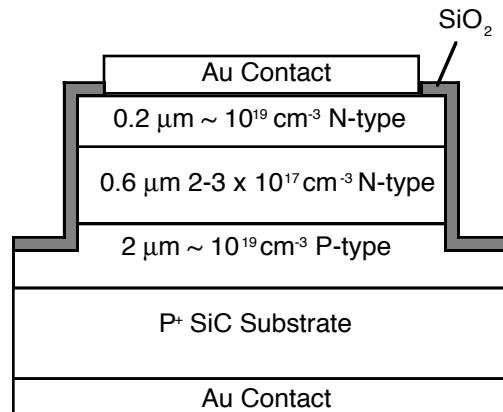


Fig. 1. 4H- and 6H-SiC pn Junction Diode Cross-Section.

and typical semi-logarithmic scale reverse characteristics are shown in Figure 2. Since crystal defect densities of SiC epilayers on commercial wafers are known to be on the order of 10^4 cm^{-2} , only devices with areas less than $5 \times 10^{-5} \text{ cm}^2$ were selected for this work, so that around half should be free of micropipes and dislocations (Wang et al., 1994). Furthermore, any diode showing dc characteristics that deviated in leakage current or sharpness of breakdown knee from the Fig. 2 characteristics was thrown out from the working data set presented in this paper. These dc-measured breakdown voltages are consistent with comparably-doped SiC pn junction breakdowns reported in the literature (Edmond et al., 1991; Palmour et al., 1994). The temperature variation of the dc-measured breakdown voltage is presented later in Fig. 5. It should be noted that the 4H diodes exhibited a small increase in dc breakdown voltage at high temperatures, while the 6H devices exhibited an unambiguous negative temperature coefficient of dc breakdown voltage.

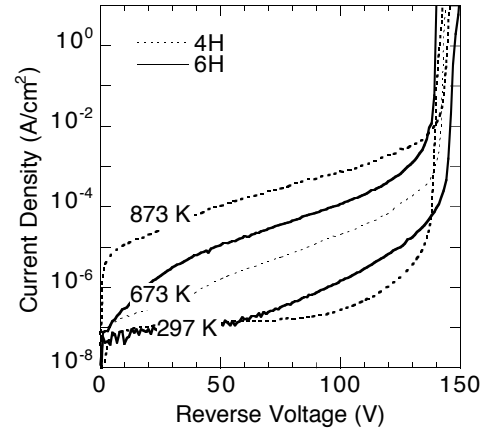


Fig. 2. DC Reverse I-V Characteristics.

Pulse Testing

Pulse bias testing was carried out using a conventional charge line circuit which nominally stressed the device under test with rectangular-shaped pulses of 200 ns width (with ~ 1 ns risetime/falltime) on a manually triggered single-shot basis. The input voltage pulse to the device under test was formed by the discharge of a semirigid coax cable through a momentarily triggered mercury vapor switch. Device voltage and current waveforms were simultaneously recorded and stored for each applied pulse using a dual-channel digitizing oscilloscope. Following digital storage of the device's voltage and current waveforms recorded with each shot, the dc I-V characteristics of the diode were re-checked with a curve tracer. The procedure was repeated with increasing pulse amplitudes until diode damage was observed by a change in the dc I-V characteristics.

Figures 3 and 4 compare room-temperature pulse-test data recorded from similarly-rated (~ 150 V, ~ 10 mA dc) 4H-SiC and silicon pn diodes, respectively. The SiC data in Fig. 3 is representative of all pulse data collected on some 20 SiC diodes of both polytypes over the entire 298 K to 873 K temperature range investigated. As expected, displacement current spikes associated with the rising and falling edges of the voltage pulse are observed, as well as non-ideal transmission-line reflection effects apparent in the 200 to 600 ns timerange. The pulsed results in Figs. 3(a & b) & 4(a) are consistent with the measured dc I-V data in that there is no detectable conduction current and the amplitude of the device voltage waveform matches the input voltage pulse amplitude. However, when the input pulse amplitude was increased to 94 V for the SiC diode (Fig. 3(c)), the collapse in measured voltage coupled with the drastic increase in conduction current indicates that the SiC device failed catastrophically less than 20 ns into the pulse. The pulse-induced catastrophic failure of the SiC diode, which was confirmed by curve-tracer measurement following the Fig. 3(c) pulse, is anomalous, since the dc-measured current (Fig. 2) at 100 V was less than $1 \mu\text{A}$. Microscopic examination of all failed SiC devices revealed highly localized damage to the device mesa and contact. This strongly suggests that a current-filamentation type failure occurred in the bulk of the device (Ridley, 1963; Shaw et al., 1992). When a filament occurs, the current density in a localized spot drastically increases, greatly stressing the junction material often to the point of failure.

In sharp contrast to the SiC diode which failed at a pulse amplitude around 70% of its dc-measured breakdown voltage, the silicon diode (Fig. 4) is able to sustain pulse amplitudes of 150% (225 V) of its dc-measured breakdown voltage. The Fig. 4 data exhibits the highly stable reverse breakdown behavior that helps make silicon power devices highly reliable (Bell Laboratories, 1984; Ricketts et al., 1976). The measured voltage across the diode in Fig. 4(c) is clamped in the neighborhood of 150 V, despite the fact that the input pulse amplitude (which can be measured open circuit when no device under test is present) had been increased to 225 V. Furthermore, positive temperature coefficient of breakdown voltage is clearly evidenced in Fig. 4(c) by the current flow decrease and device voltage increase as the device heats up over the 200 ns pulse. Because current flow decreases as junction temperature rises, the property of positive temperature coefficient of breakdown voltage in silicon junctions prevents the formation of damaging high-current filaments at junction hot-spots. Diode failure occurs at $t = 40$ ns in Fig 4(d), as clearly evidenced by the voltage collapse and sharp current increase.

The general behavior shown in Fig. 3 was observed for all SiC diodes tested at temperatures of 298 K, 473 K, 673 K, and 873 K in both 4H and 6H polytypes. The pulse amplitude at which catastrophic failure occurred is plotted as a function of temperature in Fig. 5, along with dc-measured breakdown voltages. All SiC devices failed catastrophically at pulse amplitudes that were substantially smaller than the dc-measured breakdown voltage.

DISCUSSION

Proposed Instability Mechanism

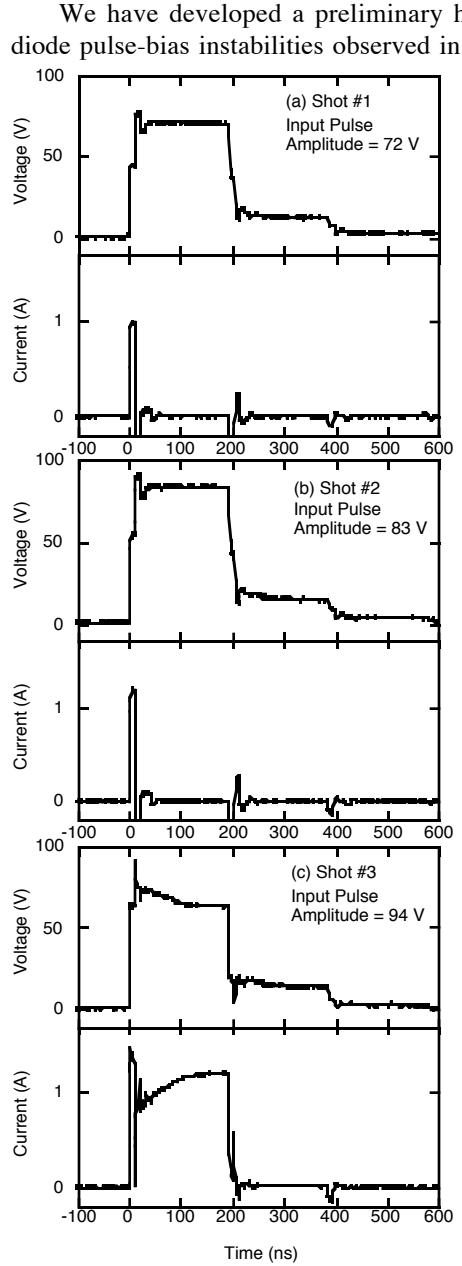


Fig. 3. 4H-SiC Diode Pulse-Test Waveforms, $T = 298\text{K}$.

We have developed a preliminary hypothesis to explain the SiC diode pulse-bias instabilities observed in this work. There is extensive literature on the physics of breakdown in semiconductors, specifically the breakdown behavior of silicon pn junctions (Bell Laboratories, 1984; Ricketts et al., 1976; Shaw et al., 1992). A significant difference between Si and SiC is that in most silicon devices, it is taken for granted that all carriers are fully ionized over the normal operational temperature range. In SiC however, the dopants are energetically deep enough that a non-trivial percentage are un-ionized at room temperature resulting in their exclusion from the transport process. Also, SiC crystal growth technology is not yet mature, resulting in the presence of deep-level centers (Mazzola et al., 1994; Pensl and Choyke, 1993). We believe that deep levels and/or incomplete ionization of dopants contribute to the unstable SiC breakdown behavior observed in this work.

For simplicity, only donor-like centers and electrons in a partially frozen-out n-type region of a junction will be considered in the following discussion. Nevertheless, the basic mechanism can also be applied to various permutations of centers (donor-like and acceptor-like) and carriers in any rectifying junction.

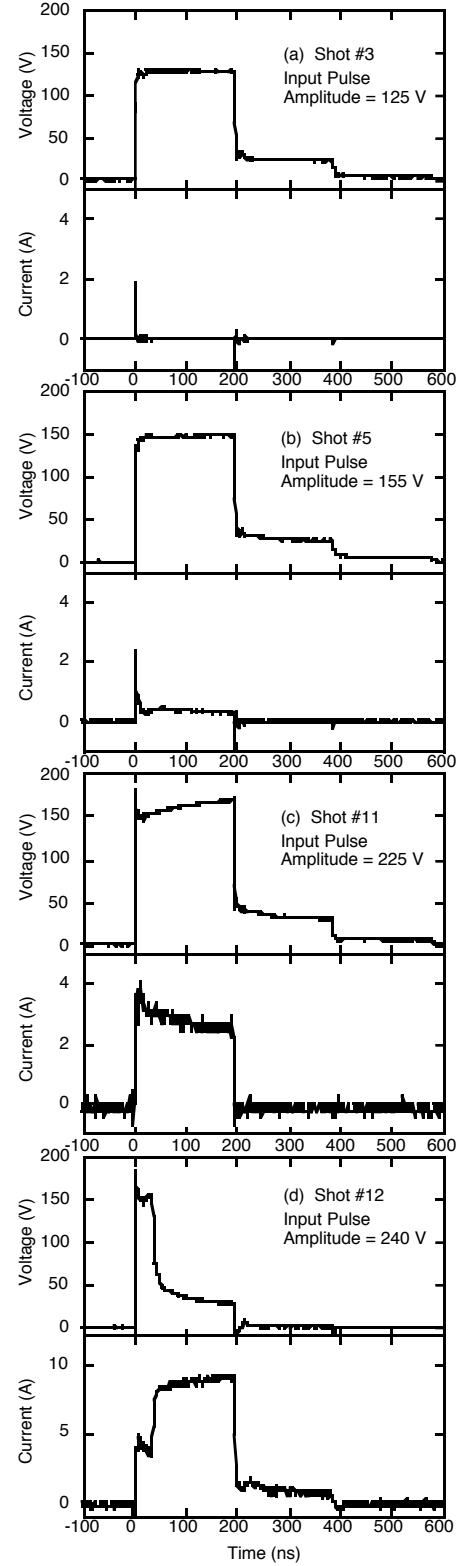


Fig. 4. Silicon Diode Pulse-Test Waveforms, $T = 298\text{K}$.

Before applying reverse bias to the SiC sample, a substantial number of carriers occupying un-ionized donors and deep-level defects in quasi-neutral regions near the depletion region edge. When a fast-risetime bias pulse is applied, the emission of trapped carriers does not occur quickly enough to keep up with the expanding depletion region. A significant percentage of carriers remain briefly trapped in the high-field depletion region at $t = 0^+$. These carriers thermally emit into the high-field depletion region at the worst time causing an undesired current surge that fails the diode. At high enough bias levels this mechanism is inferred to be a current filamentation mechanism, because the devices failed as short-circuits and post-failure inspections revealed highly localized damage within the bulk diode area. As discussed by Ridley (1963) and others (Shaw et al., 1992), current filamentation occurs when a semiconductor exhibits S-shaped negative differential conductivity (SNDC). The notion that carrier emission from deep levels and frozen-out dopants can lead to SNDC, negative temperature coefficient of breakdown, and catastrophic current filamentation failure has been previously put forth in the literature (Ridley, 1963; Scholl, 1982; Shaw et al., 1992). Given that carrier emission increases with temperature, it is possible to envision filamentation when trapped carriers emit directly into the high-field region of a near-breakdown biased junction. Localized heating at a hotspot causes remaining trapped carriers to emit even faster, causing more current and impact ionization at a junction hotspot. Even though a more rigorous examination of this phenomenon is clearly in order (such as high-field transport modeling), this initial speculative hypothesis can nevertheless serve as a starting point for more comprehensive investigations into the observed fast-risetime pulse breakdown instabilities.

The catastrophic filamentation failure mechanism does not take place in the dc steady state case, because the bias increase is over a long enough time period (16 ms on the curve-tracer) that most carrier ionization can take place in an orderly fashion near the low-field edge of the expanding depletion region in relative sync with the bias signal. The fact that the diodes were so well-behaved when dc tested suggests that leakage effects from crystal defects and junction perimeter sidewalls are probably not major contributors to the anomalous pulse-bias breakdown.

Prospects for Reliably Stable SiC Breakdown

The physical mechanisms proposed above as the primary explanation of the observed unstable SiC breakdown behavior may not necessarily be inherent to all SiC devices. Elimination of trapped carrier emission processes should result in reliable behavior from devices that are free of crystal defects. Carrier emission from deep levels will have to be eliminated by improvements to epitaxial crystal growth technology. Carrier emission from dopant sites may also need to be minimized by choosing dopants with the lowest ionization energy levels. Since conventional silicon dopants are completely ionized over the entire U.S. military specification temperature range (218 K to 398 K), carrier emission from dopant sites has never been an important mechanism in the high-field behavior silicon junctions. However in wide-bandgap semiconductors such as 4H- and 6H-SiC, a significant percentage of dopants are frozen-out around room temperature, so that carrier emission from dopant sites could perhaps contribute to the unstable breakdown behavior. Since percent ionization increases as doping decreases, SiC devices with lighter dopings than those employed in this work might be more likely to exhibit stable reverse breakdown behavior, if crystal defects and deep levels are sufficiently low. After our pulse-test circuitry is improved to enable larger pulse amplitudes, we plan to investigate a variety lighter-doped (higher voltage) SiC samples.

In the absence of extensive experimental pulsed breakdown data for a variety of SiC devices, it is difficult to quantitatively ascertain the dopings and temperatures under which SiC might achieve a stable avalanche breakdown. Nevertheless, if one were to make an educated guess that a semiconductor needed to be at least 90% ionized in order to achieve avalanche stability, one could employ standard equilibrium carrier statistics calculations (Sze, 1981) to obtain a rough first estimate of the doping-temperature space over which wide-bandgap semiconductor junctions should theoretically have stable breakdown properties. We have constructed such a plot for 4H- and 6H-SiC in Figure 6. Since elimination of both dopant and deep-level carrier emission processes may be necessary, we have plotted the estimated regions of breakdown stability based on three common SiC impurities: nitrogen (intentional n-dopant), aluminum (intentional p-dopant), and the boron-related D-center (residual deep-level contaminant). For multi-level

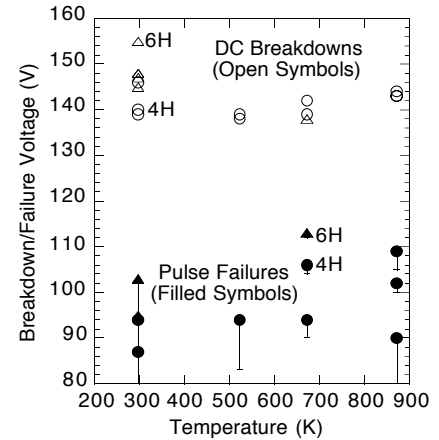


Fig. 5. DC Breakdown Voltage and Catastrophic Pulse Failure Voltage as a Function of T.

impurities, the calculations of Fig. 6 are based solely on the energetically deeper levels of the particular impurity, since the deeper level will contain the most un-ionized carriers at equilibrium. Therefore, ionization energies of 0.1 eV and 0.145 eV for nitrogen in 4H and 6H (respectively), 0.2 eV for aluminum, and 0.6 eV for the D-center (Pensl and Choyke, 1993) were used to construct the regions of unconditional breakdown stability shown in Fig. 6. The lines for each dopant species represents where the equilibrium deeper-energy impurity is theoretically 90% ionized. Therefore, a junction with doping and temperature that lie in the region well above the 90% line could be expected to exhibit unconditionally stable silicon-like avalanche breakdown behavior, while junctions that lie well below the 90% ionization lines would not exhibit unconditional breakdown stability. For example, if a 4H-SiC power diode is to exhibit unconditional breakdown stability at 218 K (-55 °C, U.S. military specification), Fig. 6 predicts that somewhere around $7 \times 10^{15} \text{ cm}^{-3}$ would be the maximum n-type doping that could be employed in the high-field region of the device. As one would intuitively expect, the shallowest impurity (nitrogen) results in the largest doping-temperature region of unconditional breakdown stability in Fig. 6 for both polytypes, while the deepest impurity (the D-center) leads to the smallest theoretical breakdown stability region. Fig. 6 is admittedly a simplistic first-order estimation, since it ignores device-specific geometry, neglects self-heating effects, doesn't account for compensation, considers only one level of multi-level centers, and is based upon an unproven 90% ionization stability criterion. Nevertheless, Fig. 6 can serve as an initial starting point for envisioning the temperature-impurity conditions under which 4H- and 6H-SiC diodes might exhibit unconditionally stable reverse breakdown behavior.

It is possible that a device without deep levels whose doping lies somewhat below the 90% dopant ionization line might exhibit partially stable (conditionally stable) breakdown behavior, in that the device could conceivably self-heat itself into stability before a destructive current density is reached within a current filament. A conditionally stable device might prove sufficiently reliable for high-power electronics, provided that its contact metallizations could withstand the high localized current densities and temperatures of the brief beginnings of current filaments.

Clearly, a more thorough experimental investigation of the pulse-breakdown behavior of SiC diodes is needed. Such an investigation could not only verify or refute the pulse-breakdown instability mechanism proposed above, but it could also ascertain the conditions under which SiC junctions exhibit reliably stable reverse breakdown behavior.

CONCLUSION

The importance of this work is best summarized by the contrasting pulse-testing results between silicon and SiC diodes that exhibit comparable dc breakdown voltages around 150 V. When subjected to fast-risetime bias pulses, the SiC diode fails at pulse amplitudes of around 100 V, while the silicon diode can withstand pulse amplitudes of over 225 V. The particular SiC devices tested above cannot be considered reliable if a single impulse glitch of modest voltage can catastrophically fail every diode within a few nanoseconds. Since impulse glitches occur in many kinds of power systems, it is unlikely that SiC power diodes exhibiting the unstable breakdown properties observed in this work could be operated reliably in a system at bias points anywhere near the dc breakdown voltage the way that silicon diodes are routinely operated. Furthermore, circuits would have to be carefully designed to insure that unstable SiC diodes would never see a single impulse glitch of sufficient amplitude to cause failure. Whether this involves the use of additional protection circuitry, or significant device voltage derating, or both, it is likely that there will be a significant performance, cost, and/or reliability penalty associated with compensating power circuits for unstable device breakdown behavior. We have shown that the safe reverse voltage rating of a SiC power device should not be solely based upon its curve-tracer measured reverse knee voltage. If SiC power devices are to replace silicon devices in power system circuits, the unreliable breakdown behavior reported in this paper must be eliminated. We propose that reliable SiC junction breakdown behavior can be achieved by eliminating or minimizing carrier emission from deep levels and/or un-ionized dopants.

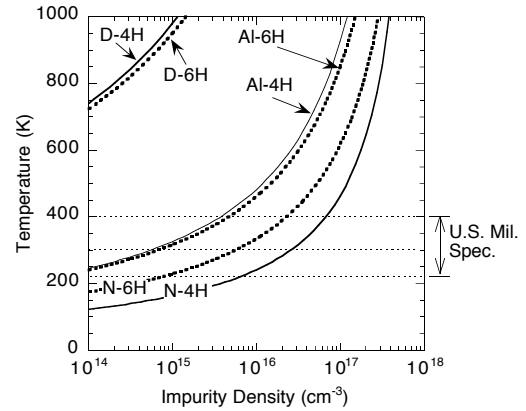


Fig. 6. Doping-Temperature Regions of 90% Ionization for Unconditional Breakdown Stability Criterion.

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